DECLARATION

I, the undersigned, Shoji EGUCHI, c/o NEC Electronics Corporation, of 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa 211-8668, Japan, do hereby solemnly and sincerely declare that I am familiar with the English and Japanese languages, that I have prepared the attached English translation which is a full, true and faithful one of the patent application filed with the Patent Office of Japan under the Application No. 026485/2003 and that the present declaration is intended for use in connection with a patent application placed before the United States Patent and Trademark Office.

I further declare that all statements made herein in my own knowledge and belief are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issuing thereon.

(Shoji EGUCHI)
c/o NEC Electronics Corporation

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[Title of the Invention] Semiconductor Device and Method of Manufacturing the Same

[Scope of Claims]

[Claim 1]

A semiconductor device including a semiconductor chip connected to a wiring board through flip chip bonding, an underfill resin reinforcing the semiconductor chip, a reinforcement frame (stiffener) surrounding the semiconductor chip, and a lid attached to a back surface of the semiconductor chip and a top of the reinforcement frame (stiffener),

the semiconductor device characterized by comprising two layered resins which are the underfill resin and a gap resin, the underfill resin being filled in an interstice between the semiconductor connected to the wiring board through flip chip bonding and the wiring board, and a gap resin being filled in a gap between a fillet extending from the underfill and the lid.

[Claim 2]

A semiconductor device including a semiconductor chip connected to a wiring board through flip chip bonding, an underfill resin reinforcing the semiconductor chip, a reinforcement frame (stiffener) surrounding the semiconductor chip, and a lid attached to a back surface of the semiconductor chip and a top of the reinforcement frame (stiffener),

the semiconductor device characterized in that

a gap resin is filled in an interstice between an inner side of the reinforcement frame (stiffener) and a fillet extending from an underfill which is formed in a way that the underfill surrounds an outer periphery of the semiconductor chip, the gap resin having a coefficient of thermal expansion smaller than that of the underfill resin, and

the underfill resin of the same type is filled in an interstice between

the wiring board and the semiconductor chip so that the wiring board and the semiconductor chip are adhered to each other therewith, and the underfill resin of the same type is filled in an interstice between the wiring board and the frame-shaped reinforcement frame (stiffener) so that the wiring board and the frame-shaped reinforcement frame (stiffener) are adhered to each other therewith.

[Claim 3]

A semiconductor device including a semiconductor chip connected to a wiring board through flip chip bonding, an underfill resin for reinforcing the semiconductor chip, a reinforcement frame (stiffener) surrounding the semiconductor chip, and a lid attached to a back surface of the semiconductor chip and a top of the reinforcement frame (stiffener),

the semiconductor device characterized in that

a gap resin is filled in an interstice between an inner side of the reinforcement frame (stiffener) and a fillet extending from the underfill which is formed in a way that the underfill surrounds an outer periphery of the semiconductor chip, the gap resin having a coefficient of thermal expansion smaller than that of the underfill resin, and

another gap resin is formed so as to extend outwards from each of four corners of the semiconductor chip in an interstice between the framed-shaped reinforcement frame (stiffener) and the wiring board.

[Claim 4]

The semiconductor device as recited in claim 3, characterized in that the thickness of an adhesive with which to adhere the reinforcement frame (stiffener) and the wiring board is a mixture of thicker portions and thinner portions.

[Claim 5]

The semiconductor device as recited in any one of claims 3 and 4,

characterized in that the adhesion surface where the reinforcement frame (stiffener) and the wiring board are adhered to each other is a mixture of convex surface portions and concave surface portions.

[Claim 6]

The semiconductor device as recited in any one of claims 3 to 5, characterized in that the reinforcement frame (stiffener) and the wiring board are connected to each other with an alloy (solder) having a low melting point used in the convex surface portions and with the underfill resin used in the concave surface portions.

[Claim 7]

The semiconductor device as recited in claim 3, characterized in that the reinforcement frame (stiffener) and the wiring board are connected to each other with the gap resin used along the diagonal lines of the reinforcement frame (stiffener) and with an adhesive used along the four sides of the reinforcement frame (stiffener), the adhesive being other than the gap resin, and the four sides being other than portions where the gap resin is used.

[Claim 8]

The semiconductor device as recited in any one of claims 3 and 7, characterized in that the reinforcement frame (stiffener) has grooves which are formed along the diagonal lines thereof.

[Claim 9]

The semiconductor device as recited in any one of claims 1 to 3, characterized in that

the fillet is that which extends in the shape of a parabola at least from a lower part of the sidewall surface of the semiconductor device to the surface of the wiring board, and

the gap resin is in contact with the inner wall of the reinforcement

frame (stiffener) and the lid, the inner wall of the lid, the fillet, the wiring board and the sidewall of the semiconductor chip.

[Claim 10]

The semiconductor device as recited in any one of claims 1 to 3 and claims 8 to 9, characterized in that the gap resin has a coefficient of thermal expansion which is smaller than that of the underfill resin.

[Claim 11]

The semiconductor device as recited in any one of claims 1 to 3 and 8 to 10, characterized in that a resin having an elastic coefficient which is larger than that of the underfill resin is used as the gap resin.

[Claim 12]

The semiconductor device as recited in any one of claims 1 to 8, characterized in that the reinforcement frame (stiffener) is made of any one of Cu, SUS, alumina, silicon and a resin.

[Claim 13]

The semiconductor device as recited in any one of claims 1 to 3, 7, and 9 to 11, characterized in that a resin essentially containing any one of epoxy, polyolefin, silicone, cyanate ester, polyimide, and polynorbornane materials is used as each of the underfill resin and the gap resin.

[Claim 14]

A method of manufacturing the semiconductor device as recited in claims 1 to 3, characterized by comprising the steps of:

adhering the reinforcement frame (stiffener) to the wiring board;

connecting the semiconductor chip to the wiring board;

filling and hardening the underfill resin therein;

filling and hardening the gap resin therein;

attaching the lid thereto; and

connecting solder bumps thereto,

the method of manufacturing the semiconductor device, characterized in that

at least the step of adhering the reinforcement frame (stiffener) to the wiring board is used as a first step to be performed, and

the step of connecting the semiconductor chip to the wiring board is used a second step to be performed.

[Claim 15]

The method of manufacturing the semiconductor device as recited in claim 13, characterized in that

the step of adhering the reinforcement frame (stiffener) to the wiring board, the step of connecting the semiconductor chip to the wiring board, the step of filling and hardening the underfill resin and the step of filling and hardening the gap resin are those in which the respective resins are half-hardened, and

the resins are fully hardened in a hardening process performed in the step of attaching the lid thereto.

[Claim 16]

The method of manufacturing the semiconductor device as recited in claim 3, characterized by comprising the steps of:

adhering the reinforcement frame (stiffener) to the wiring board;

connecting the semiconductor chip to the wiring board;

filling and hardening the underfill resin therein;

filling and hardening the gap resin therein;

attaching the lid thereto; and

connecting solder bumps thereto,

the method of manufacturing the semiconductor device, characterized in that the step of filling and hardening the gap resin therein is performed after the step of attaching the lid thereto.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention Pertains]

The present invention relates to a semiconductor device in which a semiconductor chip is connected, through flip chip bonding, to a wiring board manufactured with the same method as the a printed board is manufactured, and relates to a method of manufacturing the same.

[0002]

[Prior Art]

In general, a wiring board to which a semiconductor chip is connected through flip chip bonding is manufactured with the same method as an organic printed wiring board. The wiring board is formed of two up to ten-odd layers depending on purposes. Although the wiring board is formed of up to ten-odd wiring layers, the wiring board has a thickness of 0.5 mm to 2.0 mm. As a result, the wiring board is very vulnerable to external force and stress stemming from difference in thermal expansion among materials of different kinds, and accordingly is prone to deform. Outside dimensions are different to a large extent from one wiring board to another depending on the size of semiconductor chips mounted on the semiconductor device, the number of external terminals, and a type of layout of the external terminals, for example, whether the layout is of a full-grid type or of a peripheral-grid type.

For example, a semiconductor device takes an external shape of a square with 45 mm to 50 mm in side length, and has a thickness of approximately 2.5 mm, in a case where, in order to meet a requirement for a semiconductor device to be formed thinner and lighter in weight, the semiconductor chip is a square of approximately 17 mm to 20 mm in side length, the number of pad electrodes is 500 to 800, and the type of layout of

1800 to 2000 external terminals (bumps) in the wiring board is the full-grid.
[0003]

First of all, descriptions will be provided for a conventional semiconductor device by use of Patent Document 1 and Figs. 14 to 21.

In a case of a semiconductor device disclosed in Patent Document 1, a semiconductor chip 2 is connected, through flip chip bonding, to a wiring board 1 with a thickness of approximately 1 mm. Subsequently, an underfill resin 6 is filled to the interstice between the semiconductor chip 2 and the wiring board 1, and the resin is hardened. Thereafter, for the purpose of adhering a lid 12 to the resultant wiring substrate 1, a reinforcement frame (stiffener) 7 is adhered thereto in a way that the reinforcement frame surrounds the circumference of the semiconductor chip 2, and the lid 12 is fixed to the back surface of the semiconductor chip 2 and the surface of the reinforcement frame (stiffener) 7 by use of a conductive adhesive 9.

Fig. 14 is a plane view of the conventional semiconductor device from which the lid 12 is removed. A gap 17 is formed between the reinforcement frame (stiffener) 7 and the sides of the semiconductor chip 2.
[0004]

Descriptions will be provided for a manufacturing method by referring to Figs. 15(a) to 15(e) and Figs. 16(f) to 16(g).

First of all, the wiring board 1, the semiconductor chip 2, the reinforcement frame (stiffener) 7, the underfill resin 6, an epoxy resin adhesive 10, a conductive adhesive 9 and the lid 12 are prepared, and the wiring board shown in Fig. 15(a) is set on a stage (not illustrated) of a screen printer or a dispenser. Subsequently, the epoxy resin adhesive 10, in which the concentration of the epoxy resin is 16 ppm to 22 ppm, is applied to a periphery of the wiring board 1 by means of the screen printer or the

dispenser. Thereafter, the reinforcement frame (stiffener) 7 is placed on the applied epoxy resin adhesive 10, and is cured at a temperature of approximately 100 °C. As shown in Fig. 15(c), pads of the semiconductor chip 4 and lands of the wiring board 1 are aligned with each other by means of a flip chip mounter (not illustrated). In a case where the pads are made of an alloy with a low melting point, for example, a Pd-free solder, the pads are melted, and thus the semiconductor chips 2 and the wiring board 1 are joined to each other.

[0005]

The following method is used as another method of joining the pads of the semiconductor chip 4 and the lands of the wiring board 1 to each other. The material for one joint surface is made of Au and Al, and the material for the other joint surface is made of Au and Au. Such joint surfaces are joined to each other by applying ultrasonic waves to the surfaces while heating the surfaces. In this case, the epoxy resin adhesive 10 for the reinforcement frame (stiffener) 7 is fully cured in another step. Subsequently, for the purpose of securing the adhesive strength between the wiring board 1 and the semiconductor chip 2, the underfill resin 6 which has a 32-ppm coefficient of thermal expansion, and which is flowable, is filled in the interstice between the surfaces which is approximately 100 μm in width by means of the dispenser or the like through capillary attraction. Thereafter, the underfill resin 6 is cured at a temperature of approximately 100°C.

[0006]

After that, in a step shown in Fig. 15(e) on the back surface of the semiconductor chip 4, the conductive adhesive 9 with a coefficient of thermal expansion of 16 ppm to 22 ppm is applied to tops of the reinforcement frame (stiffener) 7 and the semiconductor chip 2. Otherwise the conductive adhesive 9 is adhered to the tops of the reinforcement frame (stiffener) 7 and

the semiconductor chip 2 by a printing method. Subsequently, in a step shown in Fig. 16(f), the lid 12 is aligned with the reinforcement frame (stiffener) 7, and the conductive adhesive 9 is simultaneously hardened at a temperature of approximately 150 °C to 170 °C while the lid 12 is being pressed against the reinforcement frame (stiffener) 7. Generally-used method for the curing include a method of applying a batch process to the conductive adhesive 9 in an oven, and a method of curing the conductive adhesive 9 by successively placing the conductive adhesive 9 to a belted furnace.

[0007]

Finally, Fig. 16(g) shows the state of the resultant wiring board whose temperature returns to normal temperature after the solder bumps which are the external terminals are adhered to the lands of the wiring board by one of the generally-used methods for the curing. While the resultant wiring board is in this state, the wiring board is already pulled towards the tip by a distance of about 100 μm, and accordingly the wiring board is shaped like a convexity which juts up. Fig. 16(g) does not show the state of the resultant wiring board, but the shape of the wiring board changes as shown by a dashed line in Fig. 20(a).

[0008]

Fig. 17(a) shows how the wiring board warps at normal temperature equal to 20°C when a temperature cycle is repeated from normal temperature, a low temperature of minus 45°C to normal temperature, a high temperature of 150°C to normal temperature. Fig. 17(b) shows how the wiring board warps at minus 45°C when the temperature cycle is repeated. Fig. 17(c) shows how the wiring board warps at 150°C when the temperature cycle is repeated. The wiring board extends up toward the chip by the distance of 100μm at normal temperature, as shown in Fig. 17(a).

When the wiring board being in this state is cooled down to minus 45°C, the wiring board warps to an extent equivalent to up to 180μm. When the wiring board is heated up to 150°C after the wiring board is returned from the cooling temperature to normal temperature, the extent to which the wiring board warps reduces to up to approximately 50μm. After this temperature cycle is repeated about hundreds times to one thousand times, the repetition causes a separation 15 of internal lands 4 of the semiconductor chip 2 from the wiring board, and causes a crack 16 in the solder bump, as shown in an magnified view of Fig. 19.

[0009]

This condition will be described by use of a magnified cross-sectional view of the solder bump and its surroundings, which is shown in Fig. 19. A reason why the repetition of the temperature cycle cracks the solder bump and separates the land from the wiring board can be assumed as follows. Shrinkage of the underfill resin pulls the wiring board toward the semiconductor chip, and applies a force to the wiring board in the vertical direction of the wiring board, even though the underfill resin absorbs stress applied to the wiring board in a direction parallel to the plane of the wiring board. When the temperature cycle is repeated while the wiring board is in this condition, the repetition causes the wiring board, inclusive of the semiconductor chip, to alternately take on the convex shape and the planar shape. Accordingly, pulling stress and pressing stress are alternately imposed on an electrode of the semiconductor chip of the solder bump or a land bonding portion of the wiring board. As a result, the alternate imposition leads to the destruction.

[0010]

The flip-chip semiconductor device 17 manufactured by means of the manufacturing method, which has been described above, is constructed as

follows. An interconnect electrode (not illustrated) of the resin-made wiring board 1, which has a thickness of 0.5mm to 2.0mm, is connected to the pad of the semiconductor chip 2 which has a thickness of 0.7mm. The interconnect electrode and the pad are fixed to each other with the underfill 6 which reinforces the respective bonding portions. The reinforcement frame (stiffener) 7 which has a thickness of approximately 0.5mm to 1.0mm is adhered to the wiring board in a way that the reinforcement frame (stiffener) 7 surrounds the semiconductor chip 2. This ensures the flatness and the strength of the wiring board. The lid 11 with a thickness of 0.5mm to 1.0mm is adhered to the resultant wiring board for the purposed of protecting the semiconductor chip 2.

[0011]

The wiring board of the semiconductor device manufactured by use of the foregoing construction materials warps as shown in Fig. 20(a) at normal temperature. The cross-sectional view shown in Fig. 20(a) is a cross-sectional view of the semiconductor device taken along the A-A' line of Fig. 14(b). A portion of the wiring board immediately under the semiconductor chip is pulled up towards the semiconductor chip due to the shrinkage of the underfill resin. As a result, the wiring board is shaped like the convexity extending upwards.

In addition, the wiring board changes its shape to an extent that another portion of the wiring board immediately under the reinforcement frame (stiffener) 7 is shaped like a convexity slightly extending upwards. In other words, the wiring board has the two types of warps.

[0012]

Fig. 21 is a graph showing how a conventional wiring board and the wiring board according to the present invention warp depending on the temperature cycle.

[0013]

One device for correcting this condition of the wiring board is to make the coefficient of thermal expansion of the underfill resin 6 as low as 16ppm to 22ppm. This makes it possible to prevent the portion of the wiring board immediately under the semiconductor chip from being pulled up into the shape of the convexity. However, the viscosity of the underfill resin arises so that voids are incorporated into the underfill resin. This results in the separation. Consequently, it is difficult to make the coefficient of thermal expansion of the underfill resin equal to, or lower than, 32ppm. In sum, the underfill resin has an irreconcilable property that much of filler such as silica or alumina needs to be mixed with the underfill resin for the purpose of lowering the coefficient of thermal expansion of the underfill resin whereas such mixture increases the viscosity of the underfill resin.

[0014]

[Patent Document 1]

Japanese Patent Application 2000-323624

[Patent Document 2]

Japanese Patent Application 2000-260820

[Patent Document 3]

Japanese Patent Application 2000-349203

[0015]

[Problem to be Solved by the Invention]

In the case of the conventional semiconductor device manufactured with the foregoing material configuration, the coefficient of thermal expansion and the elasticity are different from one material to another. As a result, the portion of the wiring board which is immediately under the semiconductor chip, and which is connected to the semiconductor chip, warps when the manufacturing process is completed. That is because the stress

pulling the portion towards the semiconductor chip is generated there. If the semiconductor device is attempted to be mounted in a print board by means of solder while the wiring board is left warping, the warping portion thereof fails to be adequately bonded to the print board by means of the solder. In addition, by means of solder, the bump is bonded to the materials which are different from each other in coefficient of thermal expansion. One of the materials is silicon, and the other of the materials is the resin board. For the purpose of protecting this bump lest the bump should be destructed, the difference in stress between the materials is eased by using the underfill having high expansion and high elasticity. As long as the resultant is kept at normal temperature, no problem arises. However, if the resultant is repeatedly exposed to the low temperature and the high temperature through the foregoing temperature cycle, this brings about a problem that the wiring board warps, and a problem that the solder bump and the wiring board crack.

[0016]

For example, a semiconductor device disclosed in Patent Document 2 is constructed as follows. A semiconductor chip is bonded to a wiring pattern surface. Subsequently, a first sealer (underfill resin) is introduced into the interstice between the semiconductor chip and the wiring pattern surface at a temperature of 60°C to 120 C°, and the first sealer is thereafter hardened at a temperature of 140 °C to 170 °C. After that, the sides of the semiconductor chip are sealed off with a second sealer (publicly-known fillet material).

In the case of this structure, the first sealer exists immediately under the semiconductor chip, and the second sealer is formed in the shape of a fillet. However, this structural condition cannot completely prevent shrinkage of the wiring pattern immediately under the semiconductor chip.

[0017]

A semiconductor device disclosed in Patent Document 3 has a structure which is constructed by means of a manufacturing method as follows. A semiconductor chip is connected, through flip chip bonding, to an interposer board. Subsequently, a sealing resin is filled in the interstice between the board and the semiconductor chip as well as a portion corresponding to an otherwise reinforcement frame (stiffener) by transfer mold in an integrated manner. Thereafter, a heat spreader (an equivalent to the lid) is adhered to the resultant.

A problem with this semiconductor device is as follows. In a case where a sealing resin containing a large amount of fillers is poured and filled, as the underfill resin, to the interstice between the board and the semiconductor chip as well as the portion corresponding to the otherwise reinforcement frame, the viscosity of the resin increases, and voids are incorporated into the interstice. As a result, this brings about a problem, such as occurrence of separation and cracks, which impairs reliability.

[0018]

An object of the present invention is to provide a semiconductor device having characteristics as follows. At normal temperature, a wiring board on which a semiconductor chip is sealed off warps only to a tolerable extent which allows the semiconductor device to be mounted on a print board without causing problems. In addition, while conducting a temperature cycle test, solder bumps are not separated from the board, or are not destructed. The board does not crack. As a consequence, neither the solder bumps nor the wiring board is destructed.

[0019]

[Means for Solving Problems]

The present invention as means for attaining the foregoing purpose

is carried out as a method for evenly shrinking the entire wiring board and for thus causing the wiring board not to warp. A first aspect of the present invention as the means is as follows. A resin with a low coefficient of thermal expansion is filled in the interstice between a semiconductor chip 2 and a reinforcement frame (stiffener) 7, and subsequently the resin is hardened there. A second aspect of the present invention is as follows. In the resultant obtained through carrying out the first aspect of the present invention, the material, which is used as an underfill resin, is also used as an adhesive for adhering the semiconductor chip 2 and the reinforcement frame (stiffener) 7. Thereby, the adhesive shrinks at the same ratio as the underfill immediately under the semiconductor chip shrinks. A third aspect of the present invention is as follows. In the resultant obtained through the carrying out the first aspect of the present invention, the adhesive is replaced with a gap resin for the purpose of adhering the wiring board to parts of the reinforcement frame (stiffener) 7 respectively corresponding to four corner portions of the wiring board.

[0020]

For the purpose of solving the foregoing problems, the present invention as recited in claim 1 is carried out as a semiconductor device including: a semiconductor chip connected to a wiring board through flip chip bonding; an underfill resin for reinforcing the semiconductor chip; a reinforcement frame (stiffener) surrounding the semiconductor chip; and a lid fixed to the back surface of the semiconductor chip and the top of the reinforcement frame (stiffener). The semiconductor device has two resin layers. One of the two resin layers is the underfill resin which is filled in an interstice between the wiring board and the semiconductor chip connected to the wiring board through flip chip bonding. The other of the two resin layers is a gap resin which is filled in a gap between the lid and a fillet

extending from the underfill resin.

The gap resin with a low coefficient of thermal expansion is filled in the gap which exists between the reinforcement frame (stiffener) and the semiconductor chip. The gap resin is hardened there. For this reason, while a temperature cycle test designed to expose the semiconductor device to normal temperature and a high temperature alternately is being conducted, the shrinkage and the expansion is held to a minimum. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated from the wiring board.

[0021]

The present invention as recited in claim 2 is carried out as a semiconductor device including a semiconductor chip connected to a wiring board through flip chip bonding, an underfill resin for reinforcing the semiconductor chip, a reinforcement frame (stiffener) surrounding the semiconductor chip, and a lid attached to the back surface of the semiconductor chip and the top of the reinforcement frame (stiffener). In the semiconductor device, a gap resin is filled in the interstice between the inner side of the reinforcement frame (stiffener) and a fillet extending from an underfill which is formed in a way that the underfill surrounds the outer periphery of the semiconductor chip, the gap resin having a coefficient of thermal expansion and an elasticity coefficient, both of which are respectively smaller than those of the underfill resin. In addition, the underfill resin of the same type is filled in the interstice between the wiring board and the semiconductor chip so that the wiring board and the semiconductor chip are adhered to each other therewith, and the underfill resin of the same type is filled in the interstice between the wiring board and the frame-shaped reinforcement frame (stiffener) so that the wiring board and the frame-shaped reinforcement frame (stiffener) are adhered to each

other therewith.

[0022]

The gap resin with the lower coefficient of thermal expansion is filled and hardened in the interstice between the reinforcement frame (stiffener) and the semiconductor chip. The underfill resin of the same type is filled in the interstice between the wiring board and the frame-shaped reinforcement frame (stiffener). For this reason, in a temperature cycle test, conditions in which the resins in the two interstices shrink and expand are equal to conditions in which the resin immediately under the semiconductor chip shrinks and expands. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

The present invention as recited in claim 3 is carried out as a semiconductor device including a semiconductor chip connected to a wiring board through flip chip bonding, an underfill resin for reinforcing the semiconductor chip, a reinforcement frame (stiffener) surrounding the semiconductor chip, and a lid attached to the back surface of the semiconductor chip and the top of the reinforcement frame (stiffener). In the semiconductor device, a gap resin is filled in the interstice between the inner side of the reinforcement frame (stiffener) and a fillet extending from the underfill which is formed in a way that the underfill surrounds an outer periphery of the semiconductor chip, the gap resin having a coefficient of thermal expansion and an elasticity coefficient, both of which are respectively smaller than those of the underfill resin. In addition, another gap resin is formed so as to extend outwards from each of four corners of the semiconductor chip in the interstice between the framed-shaped reinforcement frame (stiffener) and the wiring board.

[0023]

The gap resin having the lower coefficient of thermal expansion is

filled and hardened in the interstice between the reinforcement frame (stiffener) and the semiconductor chip. In addition, another gap resin is formed so as to extend outwards from each of the four corners of the semiconductor chip in the interstice between the framed-shaped reinforcement frame (stiffener) and the wiring board. For this reason, shrinkage and expansion are further suppressed, particularly, in longer portions respectively along the diagonal lines. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0024]

Furthermore, the present invention as recited in claim 4 is carried out as the semiconductor device having a structure where the thickness of an adhesive with which to adhere the reinforcement frame (stiffener) and the wiring board is a mixture of thicker portions and thinner portions.

[0025]

Conditions of the adhesive resin in the interstice between the frame-shaped reinforcement frame (stiffener) and the wiring board are equal to conditions of the adhesive resin immediately under the semiconductor chip. Thereby, shrinkage and expansion are further suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0026]

The present invention as recited in claim 5 is carried out as the semiconductor device having a structure where the adhesion surface on which the reinforcement frame (stiffener) and the wiring board are adhered to each other is a mixture of convex surface portions and concave surface portions.

[0027]

Conditions in which the frame-shaped reinforcement frame (stiffener) and the wiring board are adhered to each other can be easily made equal to adhesive conditions immediately under the semiconductor chip. As a result, shrinkage and expansion are suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0028]

The present invention as recited in claim 6 is carried out as the semiconductor device having a structure where the reinforcement frame (stiffener) and the wiring board are connected to each other with an alloy (solder) having a low melting point used in convex surface portions and with the underfill resin used in concave surface portions.

[0029]

A structure in which the frame-shaped reinforcement frame (stiffener) and the wiring board are connected to each other is completely equal to a structure where the semiconductor chip and the wiring board is connected to each other. Thereby, shrinkage and expansion are further suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0030]

The present invention as recited in claim 7 is carried out as the semiconductor device having a structure where the reinforcement frame (stiffener) and the wiring board are connected to each other with the gap resin used along the diagonal lines of the reinforcement frame (stiffener) and with an adhesive used along the four sides of the reinforcement frame (stiffener), the adhesive being other than the gap resin, and the four sides being other than portions where the gap resin is used.

[0031]

The adhesive resin used on longer portions respectively along the diagonal lines of the reinforcement frame (stiffener) is made different from the adhesive resin used in portions along the sides thereof to cope with shrinkage and expansion which causes in the interstice between the reinforcement frame (stiffener) and the wiring board. For this reason, the shrinkage and expansion are suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0032]

The present invention as recited in claim 8 is carried out as the semiconductor device having a structure where the reinforcement frame (stiffener) has grooves which are formed along the diagonal lines thereof.

[0033]

The gap resin is filled in the grooves respectively along the diagonal lines thereof. For this reason, shrinkage and expansion are suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0034]

The present invention as recited in claim 9 is carried out as the semiconductor device having a structure where the fillet is that which extends in the shape of a parabola at least from a lower part of the sidewall surface of the semiconductor device to the surface of the wiring board, and where the gap resin is in contact with the inner wall of the reinforcement frame (stiffener) and of the lid, the inner wall of the lid, the fillet, the wiring board and the sidewall of the semiconductor chip.

[0035]

The gap resin is filled and hardened in the fillet extending from the sidewall of the semiconductor chip, the inner wall of the reinforcement frame

(stiffener), and the inner wall of the lid. For this reason, shrinkage and expansion are suppressed. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0036]

The present invention as recited in claim 10 is characterized in that the gap resin has a coefficient of thermal expansion which is smaller than that of the underfill resin.

[0037]

For this reason, shrinkage and expansion are suppressed in a gap portion surrounded by the semiconductor chip, the inner wall of the reinforcement frame (stiffener), the inner wall of the lid and the wiring board. This makes it possible to prevent solder bumps from cracking, and to prevent internal lands from being separated therefrom.

[0038]

The present invention as recited in claim 11 is characterized in that a resin having an elastic coefficient, which is larger than that of the underfill resin, is used as the gap resin.

[0039]

The present invention as recited in claim 12 is characterized in that the reinforcement frame (stiffener) is made of any one of Cu, SUS, alumina, silicon and a resin.

[0040]

The present invention as recited in claim 13 is characterized in that a resin essentially containing any one of epoxy, polyolefin, silicone, cyanate ester, polyimide, and polynorbornane materials is used as each of the underfill resin and the gap resin.

The present invention as recited in claim 14 is carried out as a

method of manufacturing a semiconductor device, which is characterized by including the steps of: adhering the reinforcement frame (stiffener) to the wiring board; connecting the semiconductor chip to the wiring board; filling and hardening the underfill resin therein; filling and hardening the gap resin therein; attaching the lid thereto; and connecting solder bumps thereto. The method of manufacturing of the semiconductor device is characterized in that at least the step of adhering the reinforcement frame (stiffener) to the wiring board is used as a first step to be performed, and that the step of connecting the semiconductor chip to the wiring board is used as a second step to be performed.

[0041]

This manufacturing method makes it possible to reinforce the strength of the wiring board. As a result, facility in manipulation needed during the manufacturing steps can be improved. Concurrently, this makes it possible to suppress warp of the wiring board.

[0042]

The present invention as recited in claim 15 is carried out as the manufacturing method in which the step of adhering the reinforcement frame (stiffener) to the wiring board, the step of connecting the semiconductor chip to the wiring board, the step of filling and hardening the underfill resin and the step of filling and hardening the gap resin are those in which the respective resins are half-hardened, and in which the resins are fully hardened in a hardening process performed in the step of attaching the lid thereto.

[0043]

In the case of this manufacturing method, the resins are temporarily cured in each of the steps before the last step, and the resins are fully cured and thus completely hardened in the last step.

The present invention as recited in claim 16 is carried out as the method of manufacturing the semiconductor device as recited in claim 3, which is characterized by including the steps of: adhering the reinforcement frame (stiffener) to the wiring board; connecting the semiconductor chip to the wiring board; filling and hardening the underfill resin therein; filling and hardening the gap resin therein; attaching the lid thereto; and connecting solder bumps thereto. This manufacturing method is characterized in that the step of filling and hardening the gap resin therein is performed after the step of attaching the lid thereto.

[0044]

In the case of this manufacturing method, the gap resin 8 is poured and hardened therein after the lid 12 is attached thereto. This makes it possible to fully fill the gap resin thereinto, to prevent a space from being caused, and to suppress the change in shape of the wiring board.

[0045]

[Embodiments for Carrying out the Invention]

(First Example)

Next, descriptions will be provided for a first embodiment by referring to the drawings.

Fig. 1(a) is a cross-sectional view of a semiconductor device according to the first embodiment of the present invention. Fig. 1(b) is a plan view of the semiconductor device shown in Fig. 1, from which a lid is removed. Figs. 8(a) to 8(e) and Figs. 9(f) to 9(h) are diagrams showing steps of manufacturing the semiconductor device.

In the case of the first embodiment of the present invention, a semiconductor chip 2, an underfill resin 6 and a reinforcement frame (stiffener) 7 reduce a warp in a wiring board 1 stemming from thermal stress and mechanical stress which are generated during the manufacturing steps,

and reinforce strength of the wiring board. The semiconductor chip 2 is connected to the center of the wiring board 1 through flip chip bonding. The underfill resin 6 is that for easing stress caused in the flip chip bonding portion. The reinforcement frame (stiffener) 7 is adhered to an inner periphery of the wiring board. The first embodiment has a structure as follows. A resin 8 is filled and hardened in a gap encompassed by the inner wall of the reinforcement frame (stiffener) 7, the side wall of the semiconductor chip 2, a fillet 11 extending from the underfill resin, and a lid 12, and thus no lacuna is left in the gap. The resin filled in the gap is termed as a "gap resin." A property of this gap resin is that its expansion at a high temperature and its shrinkage at a low temperature are suppressed. That is because the resin has a coefficient of thermal expansion at least lower than that of the underfill resin 6, and because this resin is filled and hardened in the gap between the semiconductor chip 2 and the reinforcement frame (stiffener) 7. Moreover, if the coefficient of thermal expansion of the gap resin is made lower than that of an adhesive 10 and that of a conductive adhesive 9, this reduces the warp in the wiring board further.

Table 1 shows properties respectively of the underfill resin, the gap resin and the like which are used in this respect.

[0046]

Table 1 Properties of Resins

	Coefficient of Thermal Expansion	Elasticity
Adhesive for Stiffener	16 ppm to 22 ppm	11 GPa to 12 GPa
Underfill Resin	30 ppm to 32 ppm	9 GPa to 10 GPa
Gap Resin	8 ppm to 15 ppm	18 GPa to 28 GPa
Conductive Adhesive	50 ppm to 100 ppm	3 GPa to 9 GPa

Next, descriptions will be provided for the manufacturing method by

following the sequence of manufacturing steps.

[0047]

As shown in Fig. 8(a), external lands 5 electrically connected to internal lands 4 are arranged on the back surface of the wiring board 1. Subsequently, the adhesive 10 is applied to the inner periphery of the wiring board 1 as if the applied adhesive 10 were the frame of a picture, as shown in Fig. 8(b). The coefficient of thermal expansion of the adhesive 10 is approximately 16 ppm to 22 ppm, and the elasticity thereof is 11 GPa to 12 GPa. The adhesive 10 essentially contains any one of an epoxy material, a polyolefin material, a silicone material, a cyanate ester material, a polyimide material and a polynorbornane material. An adequate amount of inorganic filler is mixed in the adhesive 10 for the purpose of reconciling the coefficient of thermal expansion and the elasticity. Thereafter, the reinforcement frame (stiffener) 7 is aligned to the applied adhesive 10 on the wiring board, and the adhesive 10 is temporarily cured at a temperature of 125 °C for 15 minutes. Thus, the reinforcement frame (stiffener) 7 is adhered to the wiring board 1. The temporarily-cured adhesive 10 is not completely hardened. After that, the semiconductor chip 2 is aligned to the wiring board, as shown in Fig. 8(c). Thus, the resultant is heated at 250 °C in a nitrogen atmosphere. Thereby, the semiconductor chip 2 is connected to internal lands 4 on the wiring board 1 through flip chip bonding. Subsequently, the underfill resin 6 is poured and filled into the interstice between the semiconductor chip 2 and the wring board 1 by means of a dispenser or the like using the dispenser method. A resin to be used as the underfill resin 6 is an epoxy resin with the coefficient of thermal expansion of 32 ppm, and with the elasticity of 9 GPa. If the resin with these properties is used, the flowability is 1000 CPS to 40000 CPS (centipoises), and thus the resin can be poured and filled into the interstices without causing voids as

shown in Patent Literature 3. Thereafter, the resultant is temporarily cured at a temperature of approximately 100 °C for 10 minutes. After this temporary cure, the underfill resin is still not hardened completely. Subsequently, as shown in Fig. 8(e), the gap resin 8 is filled in a gap on the underfill resin 6 and the fillet 11 extending from the underfill resin to a vicinity of the semiconductor chip, e.g., in a gap between the reinforcement frame (stiffener) 7 and the sidewall of the semiconductor chip 2 through the injection filling method, the transfer sealing method, the dispensing method using a fluid resin, or the like. A resin to be used as the gap resin 8 is an epoxy resin with the coefficient of thermal expansion of approximately 8 ppm to 15 ppm which is smaller than that of the underfill resin, and with the elasticity of 18 GPa to 28 GPa. After the gap resin is filled in the gap, the resultant is temporarily cured at 150 °C for approximately 30 minutes. After this temporary cure, the gap resin is similarly still not hardened completely.

[0048]

Like the material for the adhesive 10, the materials respectively for the underfill resin 6, the gap resin 8, and the conductive adhesive 9 are used depending on their optimal properties obtained by changing an amount of the inorganic filler contained in their respective materials. With regard to the conductive adhesive, Ag powder, Cu powder or the like is added thereto for the purpose of further imparting thermal conductivity to the conductive adhesive.

Subsequently, the conductive adhesive 9 is applied to the back surface of the semiconductor chip 2 and the reinforcement frame (stiffener) 7, as shown In Fig. 9(f). The conductive adhesive 9 is the epoxy resin to which an adequate amount of filler, such as Ag filler and Cu filler, is added. The coefficient of thermal expansion of the conductive adhesive 9 is 50 ppm to

100 ppm. Thereafter, the lid 11 is placed on the resultant, as shown in Fig. 9(g). After that, the underfill resin 6, the gap resin 8, the conductive adhesive 9 and the adhesive 10 are heated at 175 °C for approximately 60 minutes by reducing the temperature. Thus, the resultant is fully cured, and thereby the lid is completely adhered to the back surface of the semiconductor 2 and the reinforcement frame (stiffener) 7. Concurrently, the other resins are also hardened completely. Finally, Fig. 9(h) shows the resultant semiconductor device which is returned to a condition at normal temperature after the solder bumps 19, which serves as external terminals, are bonded to the respective lands on the wiring board by means of a generally-used method.

[0049]

(Second Embodiment)

Descriptions will be provided next for a second example by use of the cross-sectional view shown in Fig. 2. The manufacturing method for the second example is the same as the manufacturing method for the first example.

The configuration for the second example is substantially the same as the configuration for the first example. The only point which makes the configuration for the second example different from the configuration for the first example is that the underfill resin 6 is used as a resin with which to adhere the reinforcement frame (stiffener) 7 to the wiring board 1.

Characteristics of the second example are as follows. A resin with a coefficient of thermal expansion of 32 ppm and with a an elasticity of 9 GPa to 10 GPa is used as the resin with which to adhere the reinforcement frame (stiffener) 7 to the wiring board 1. Thereby, an extent to which the wiring board 1 immediately under the reinforcement frame (stiffener) 7 shrinks is almost the same as an extent to which the semiconductor chip 2 shrinks. In

addition, the thickness of the underfill resin used as the adhesive 10 is approximately 20 μm to 50 μm, and the thickness is approximately half of the thickness of the underfill resin filled in the interstice between the semiconductor chip and the wiring board.

[0050]

(Third Example)

Descriptions will be provided next for a third example by use of Figs. 3(a) to 3(c). Figs. 3(a) and 3(c) are respectively cross-sectional views showing a semiconductor device according to the third example. Fig. 3(b) is a plan view showing a state in which the semiconductor device is.

The semiconductor device according to the third example has a configuration as follows. The width of an interstice in which the adhesive 10 for adhering the reinforcement frame (stiffener) 7 to the wiring board 1 is filled is equal to the width of an interstice between the semiconductor chip 2 and the wiring board 1.

If the entire adhesion surface of the reinforcement frame (stiffener) 7 is formed to include spiral grooves, latticed grooves or an alternate series of convex portions and concave portions instead of the plane, this makes it possible for the adhesion surface of the reinforcement frame (stiffener) 7 to have a condition similar to a condition immediately under the semiconductor chip. The depth of the grooves or the concave portions can be set depending on the necessity. However, it is desirable that the depth be 50 μm to 200 μm which is equal to the interstice between the semiconductor chip and the wiring board 1. Cu, SUS (a ferrite stainless steel), alumina, silicon, aluminum nitride, an epoxy resin or the like can be selected as the material for the reinforcement frame (stiffener) 7.

This reinforcement frame (stiffener) 7 is adhered to the wiring board 1 by using the underfill resin 6 as the adhesive. It goes without saying that

the adhesive used in the first example can be used for the adhesive for the third example.

[0051]

In the structure where the reinforcement frame (stiffener) 7 and the lid 12 superposed over the wiring board 1 are made of Cu, the configuration, which consists of the semiconductor chip 2, the wiring board 1, the underfill resin 6 and the gap resin, is also the same as the configuration used for the first example.

Functional characteristics, which the structure used for the third example exhibits at normal temperature and through the temperature cycle, are as follows. First of all, a warp of the wiring board 1 stemming from the reinforcement frame (stiffener) 7 is suppressed by making the condition, in which the wiring board and the reinforcement frame (stiffener) are adhered to each other, closer to the condition, in which the semiconductor chip and the wiring board is adhered to each other. Subsequently, the underfill resin 6 is filled in the interstice which is formed when the semiconductor chip 1 is connected to the wiring board 1. Thereafter, the gap-filling resin is filled in the entire gap. After that, the underfill resin and the gap-filling resin are hardened.

The filling of the gap-filling resin in the gap between the sidewall of the semiconductor chip and the reinforcement frame (stiffener) suppresses the upward and downward movement of the wiring board.

Subsequently, the convex portions, to which the reinforcement frame (stiffener) 7 made of silicon or Cu is connected, are metallized, and are activated by flux. Thus, the reinforcement frame (stiffener) 7 and the wiring board 1 are soldered to each other. In this case, the condition, in which the wiring board and the reinforcement frame (stiffener) 7 is adhered to each other, can be made equal to the condition in which the wiring board

and the semiconductor chip are adhered to each other. This makes it possible to suppress the warp of the wiring board which stems from the shrink of the wiring board.

[0052]

(Fourth Example)

A semiconductor device according to a fourth example has the same structure as the semiconductor device according to the third example, except that the opening portion of the reinforcement frame (stiffener) 7 is shaped like a reverse taper 20. Part of the reinforcement frame (stiffener) 7 overhangs the gap resin as if the part were an eave. This structure brings about an effect that the eave-shaped portion prevents the fillet and the gap resin from changing in shape to an extent to warping toward the lid. In addition, the forming of the opening portion in the shape of the eave makes it possible to reduce amounts of the resin materials which cause the expansion and the shrinkage. This brings about another effect of reducing the depressed area further.

[0053]

A method of manufacturing the semiconductor device according to the fourth example is the same as the method of manufacturing the semiconductor device according to the first example.

[0054]

(Fifth Example)

A fifth example will be described by use of Figs. 5(a), 5(b) and 6(c). Fig. 5(a) is a plan view of a semiconductor device according to the fifth example. Fig. 5(b) is a cross-sectional view of the semiconductor device taken along the A-A' line of Fig. 5(a). The semiconductor device according to this example corrects susceptibility to the influence of the expansion and the shrinkage due to the length of the diagonal lines of the rectangular

semiconductor device being longer than the length of the diagonal lines of a semiconductor device according to any other example.

[0055]

A characteristic of the semiconductor device according to this example is that a groove is provided to each of the four corners of the reinforcement frame (stiffener) 7, and that the groove takes on a shape into which the gap resin is penetrated. The underfill resin filled in the interstice between the semiconductor chip and the wiring board as well as the gap-filling resin are the same as the underfill resin and the gap-filling resin which are used for the third example. However, a limitation is imposed on the material of the reinforcement frame (stiffener) 7, and on the resin with which to adhere the reinforcement frame (stiffener) 7 and the wiring board to each other. In a case where a material, such as Al, Cu and SUS, which has a coefficient of thermal expansion almost equal to that of the wiring board, is used for the reinforcement frame (stiffener), the adhesive 10, with which to adhere the wiring board and the reinforcement frame (stiffener) to each other, is as follows. The gap resin 8 is filled in each of the four corners of the reinforcement frame (stiffener). The underfill resin is used as the adhesive with which to adhere the wiring board and each of the four sides of the reinforcement frame (stiffener).

Functional characteristics of the structure for the fourth example are as follows. The wiring board, the reinforcement frame (stiffener) and the adhesive are designed to almost agree with one another in thermal expansion characteristics. This agreement suppresses warp of the wiring board. Concurrently, the underfill resin and the gap resin suppress warp of part of the wiring board, the part being immediately under the semiconductor chip.

[0056]

In the case of a first method of manufacturing the semiconductor device having this structure, the reinforcement frame (stiffener) 7 with the grooves respectively in the corners is used in the step shown in Fig. 8(b). The reinforcement frame (stiffener) is adhered to the wiring board by applying the underfill resin 6 (which is epoxy or cyanate ester by chemical name) to the sides thereof, and by applying the gap resin 8 to the corners thereof.

[0057]

Descriptions will be provided for a second manufacturing method by use of Figs. 10(a) to 10(e) and Figs. 11(f) to 11(i). Steps shown in Figs. 10(a) to 10(d) is completely the same as the manufacturing steps for the first example, which are shown in Fig. 8(a) to 8(d). In a step shown in Fig. 10(e), a conductive adhesive 9 as follows is applied to the back surface of the semiconductor chip 2 and the reinforcement frame (stiffener) 7. An adequate amount of Ag filler, a Cu filler or the like is mixed into the conductive adhesive 9. In addition, the conductive adhesive 9 is an epoxy resin, and has a coefficient of thermal expansion of 50 ppm to 100 ppm. As shown in Fig. 10(g), the lid 11 is placed on the back surface of the semiconductor chip 2 and the reinforcement frame (stiffener) 7. The resultant is heated at 150 °C for approximately 30 minutes. Thus, the lid is temporarily cured, and is adhered thereto. A heated pressurized filling nozzle 18 is brought into contact with two corners of the package to which the lid 12 is connected, and thus the gap resin 8 is poured and filled therein. A method of filling the gap resin 8 therein while applying pressure to the gap resin by transfer mold can be also used. Finally, Fig. 11(i) shows a condition to which the resultant semiconductor device is returned at normal temperature after solder bumps to serve as external terminals are bonded to lands on the wiring board by a generally-used method.

[0058]

(Sixth Example)

In the case of the sixth example, the material for the reinforcement frame (stiffener) 7 is changed from the inorganic resin to an organic resin. Fig. 7(a) shows that the opening portion of the reinforcement frame (stiffener) 7 is formed perpendicular to the wiring board.

With regard to manufacturing steps, a resin-made reinforcement frame (stiffener) 7 is fabricated and prepared beforehand by transfer sealing, as shown in Figs. 12(a) to 12(e). The subsequent manufacturing sequence is the same as that of the first example. The adhesive 10 is applied to the wring board 1, and the resin-made reinforcement frame (stiffener) 7 is placed thereon, followed by temporary cure. Thereafter, the semiconductor chip is soldered to internal lands 4. After that, the underfill resin 6 is filled in the interstice between the semiconductor chip and the wiring board, followed by temporary cure. Subsequently, the conductive adhesive 9 is applied to the back surface of the semiconductor chip and the surface of the reinforcement frame (stiffener) 7, and the lid 12 is placed thereon, followed by full cure. Thereby, the adhesive, the underfill resin, the conductive adhesive are completely hardened. Consequently, the semiconductor device is completed.

[0059]

Another manufacturing method can be applied. In the case of this manufacturing method, the wiring board 1 is placed on a die for transfer sealing, and the resin-made reinforcement frame (stiffener) 7 is formed on the wiring board 1 in a manner that the reinforcement frame (stiffener) 7 and the wiring board 1 are integrated into a single unit. The subsequent steps of the manufacturing method are the same as those of the conventional manufacturing method. The use of this manufacturing method makes it possible to save resources in the manufacturing steps.

[0060]

(Seventh Example)

A semiconductor device according to a seventh example is the same as that according to the sixth example, except that the opening portion of the reinforcement frame (stiffener) is shaped like a reverse taper 20, and that part of the reinforcement frame (stiffener) accordingly overhangs the gap resin as if the part were an eave. This structure brings about an effect that the shape of the eave prevents the fillet and the gap resin from changing in shape. In addition, the forming of the opening portion in the shape of the eave makes it possible to reduce amounts of the resin materials, which cause the expansion and the shrink. This brings about another effect of reducing the depressed area further.

The manufacturing method of the seventh example is the same as that of the sixth example.

[0061]

As described above, in the case of the first aspect of the present invention, the semiconductor chip is connected to the wiring board through flip chip bonding. The underfill resin is filled in the interstice between the wiring board and the semiconductor chip. Subsequently, the reinforcement frame (stiffener) is adhered to the wiring board in a way that the reinforcement frame (stiffener) surrounds the semiconductor chip, and thus the resultant is used as the supporting body for the lid. In this case, the gap resin is filled in the gap encompassed by the wiring board, the semiconductor chip, the reinforcement frame (stiffener) and the lid, followed by hardening. The coefficient of thermal expansion of the gap resin is smaller than that of the underfill resin. For this reason, the gap resin makes it possible to suppress the upward and downward movement of the wiring board stemming from the expansion and the shrink. This makes it possible to

prevent the temperature cycle from cracking the solder bumps, and from separating the lands therefrom.

[0062]

The second aspect of the present invention brings about the following effects in addition to the effects brought about by the first aspect of the present invention. The underfill resin is used as the adhesive with which to the reinforcement frame (stiffener) to the wiring board. Thereby, the extent to which the wiring board immediately under the reinforcement frame (stiffener) shrinks is made equal to the extent to which the wiring board immediately under the semiconductor chip shrinks. This makes it possible to prevent the temperature cycle from cracking the solder bumps, and from separating the lands, better than the first aspect of the present invention does.

The rectangular semiconductor device conspicuously shrinks and expands along the diagonal lines thereof. That is because the rectangular semiconductor device has a larger dimension along the diagonal lines than a semiconductor device in any other shape. The third aspect of the present invention suppresses the expansion and the shrink along the diagonal lines. The gap resin with the lower coefficient of thermal expansion is used as the adhesive with which to adhere the wiring board to the four corners of the reinforcement frame (stiffener). This is the method of further suppressing the expansion and the shrink along the diagonal lines in addition to the effects brought about by the first aspect of the present invention. This makes it possible to prevent the temperature from cracking the solder bumps, and from separating the lands therefrom.

[Brief Description of the Drawings]

Fig. 1(a) is a cross-sectional view of a semiconductor device according to a first example of the present invention.

Fig. 1(b) is a plan view of the semiconductor device according to the first example of the present invention.

Fig. 2 is a cross-sectional view of a semiconductor device according to a second example of the present invention.

Fig. 3(a) is a cross-sectional view of a semiconductor device according to a third example of the present invention.

Fig. 3(b) is a plan view of the semiconductor device according to the third example of the present invention.

Fig. 3(C) is a partially-enlarged view of the semiconductor device according to the third example of the present invention.

Fig. 4 is a cross-sectional view of a semiconductor device according to a fourth example of the present invention.

Fig. 5 (a) is a plan view of a semiconductor device according to a fifth example of the present invention.

Fig. 5(b) is a partially-enlarged, cross-sectional view of the semiconductor device according to the fifth example of the present invention, which is taken along the A-A' line of Fig. 5(a).

Fig. 6 is a cross-sectional view of the semiconductor device according to the fifth example of the present invention, which is taken along the B-B' line of Fig. 5(a).

Fig. 7(a) is a cross-sectional view of a semiconductor device according to a sixth example of the present invention.

Fig. 7(b) is a cross-sectional view of a semiconductor device according to a seventh example of the present invention.

Figs. 8(a) to 8(e) are respectively diagrams showing first manufacturing steps according to the first example of the present invention.

Figs. 9(f) to 9(h) are respectively diagrams showing the subsequent first manufacturing steps according to the first example of the present

invention.

Figs. 10(a) to 10(e) are respectively diagrams showing second manufacturing steps according to the fifth example of the present invention.

Figs. 11(f) to 11 (i) are respectively diagrams showing the subsequent second manufacturing steps according to the fifth example of the present invention.

Figs. 12(a) to 12(e) are respectively diagrams showing manufacturing steps according to the sixth example of the present invention.

Figs. 13(a) to 13(e) are respectively diagrams showing manufacturing steps according to the seventh example of the present invention.

Fig. 14(a) is a cross-sectional view of a conventional semiconductor device.

Fig. 14(b) is a plan view of the conventional semiconductor device.

Figs. 15(a) to 15(e) are respectively diagrams showing steps of manufacturing the conventional semiconductor device.

Figs. 16(f) to 16(g) are respectively diagrams showing subsequent steps of manufacturing the conventional semiconductor device.

Figs. 17(a) to 17(b) are diagrams each showing a condition in which the conventional semiconductor device warps through a temperature cycle test.

Fig. 18(c) is a diagram showing another condition in which the conventional semiconductor device warps.

Fig. 19 is an enlarged cross-sectional view of a solder bump and its vicinity.

Figs. 20(a) to Fig. 20(f) show extents to which the semiconductor devices respectively according to the examples warp.

Fig. 21 is a graph showing conditions in which the conventional wiring board and the wiring board according to the present invention warp

through the temperature cycle.

[Explanation of Reference Numerals]

1 wiring board

2 semiconductor chip

3 electrode pad

4 internal land (on wiring board)

5 external land (on wiring board)

6 underfill resin

7 reinforcement frame (stiffener)

8 gap resin

9 conductive adhesive

10 adhesive

11 fillet

12 lid

13 concave portion (groove)

14 convex portion (soldered portion)

15 separation

16 cracks

17 Gap

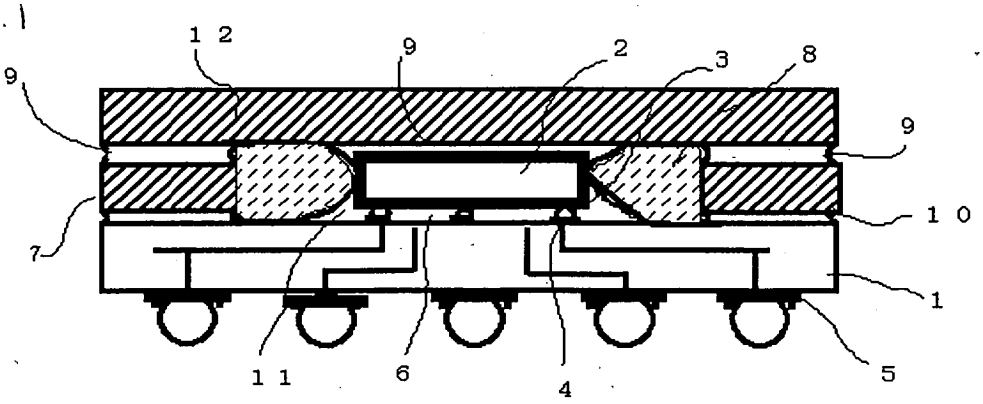
18 nozzle for pressurized filling

19 solder bump

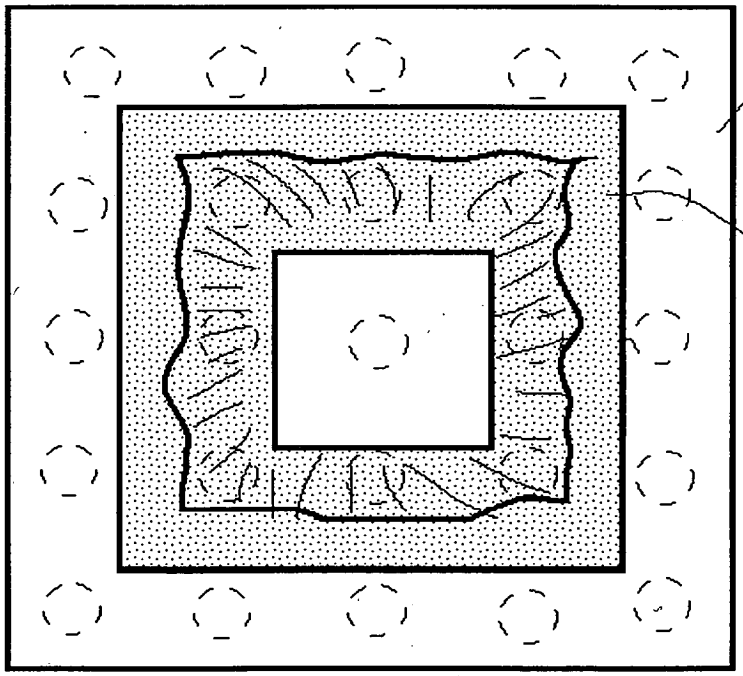
20 reverse taper

【書類名】　図面
[Document Name]　Drawings
【図１】
Fig. 1

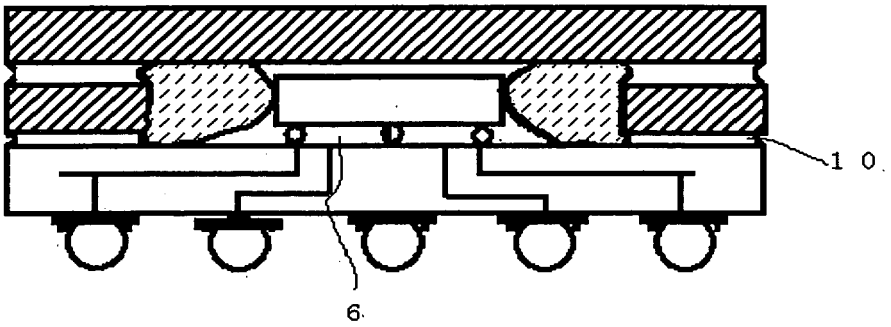
(a)



(b)

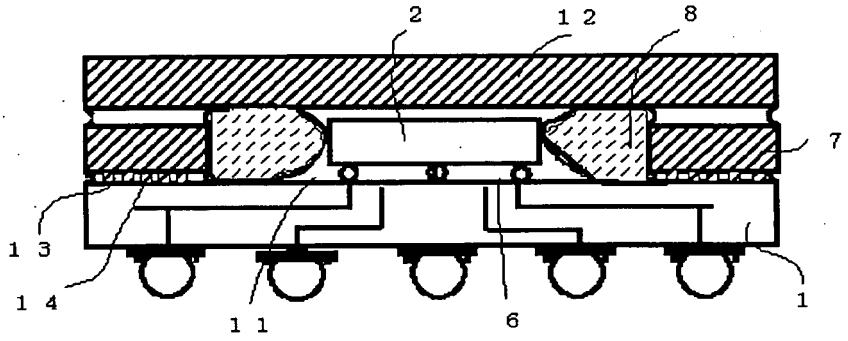


【図２】
Fig. 2

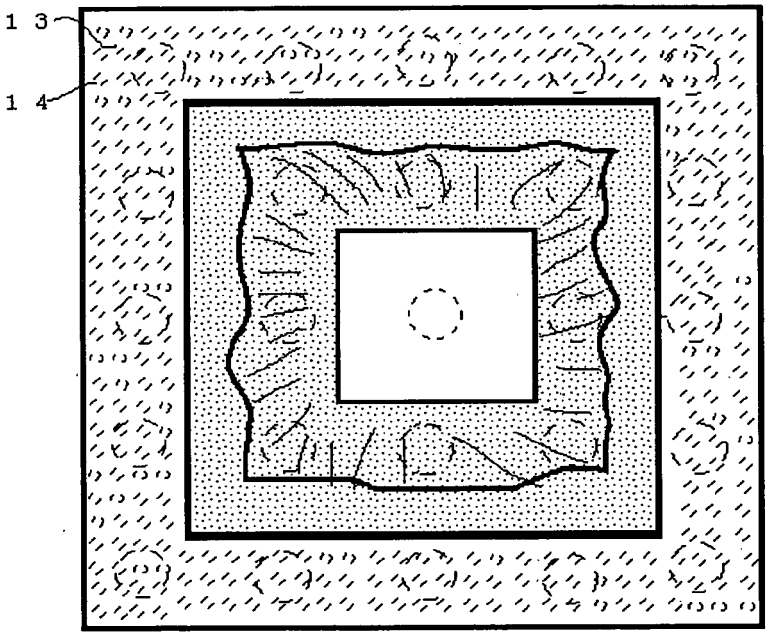


【図３】
Fig. 3

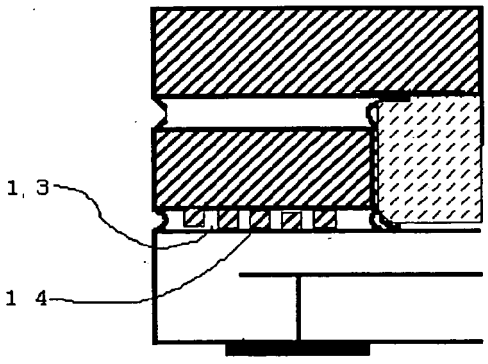
(a)



(b)



(c)



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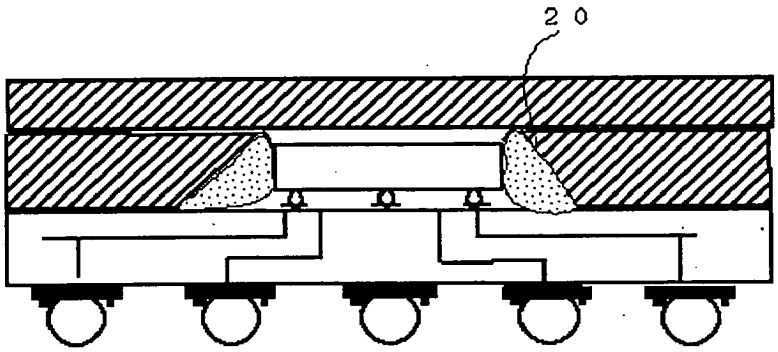
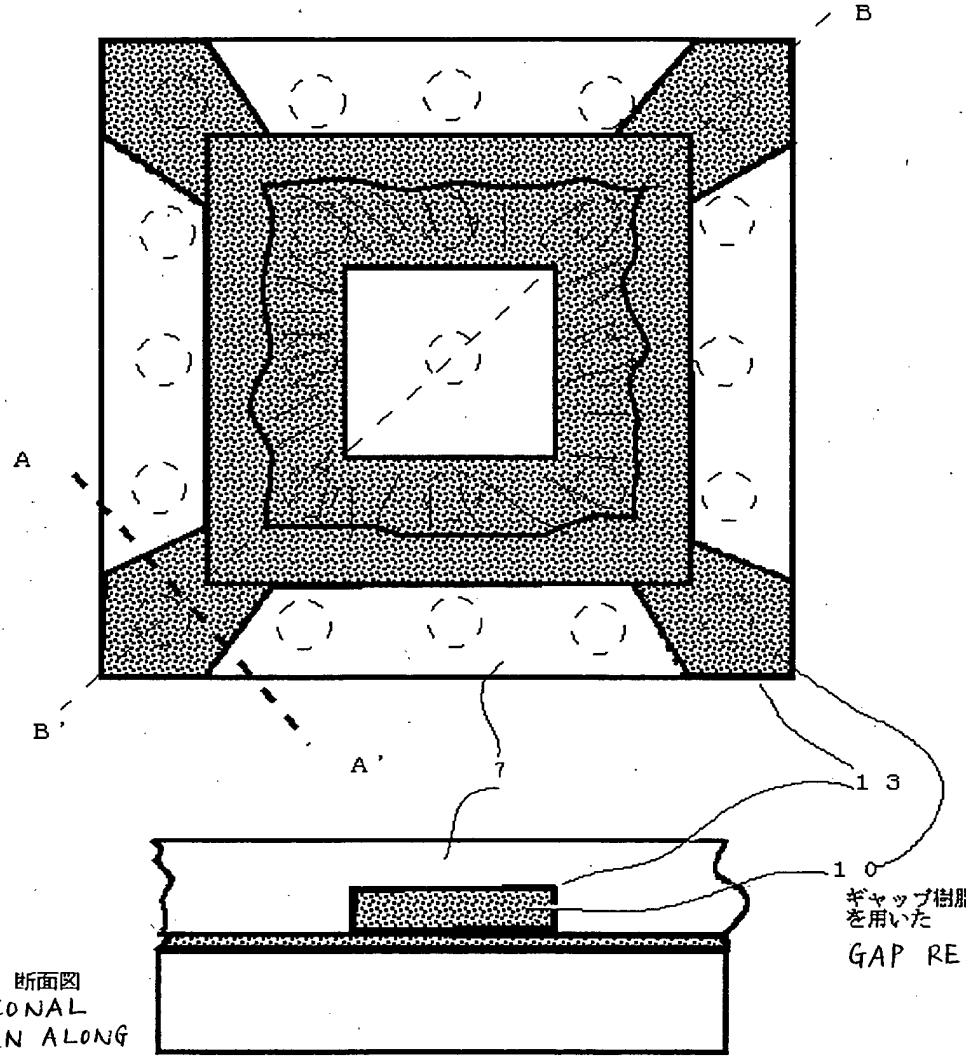
【図４】
Fig. 4



【図５】
Fig. 5



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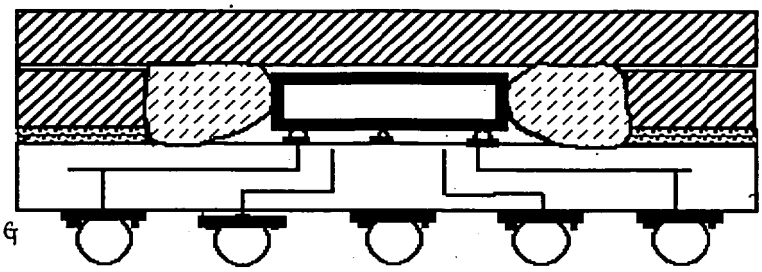
【図６】
Fig. 6

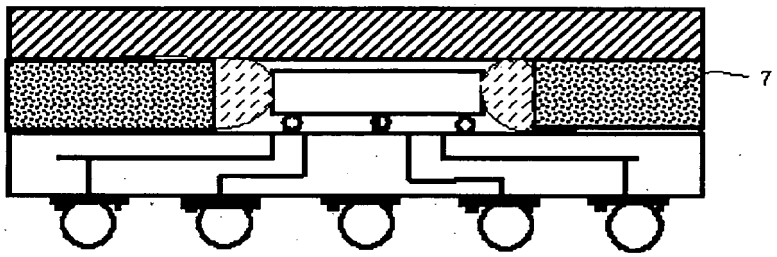
(c)

B－B' 断面図
CROSS-SECTIONAL VIEW TAKEN ALONG B－B' LINE

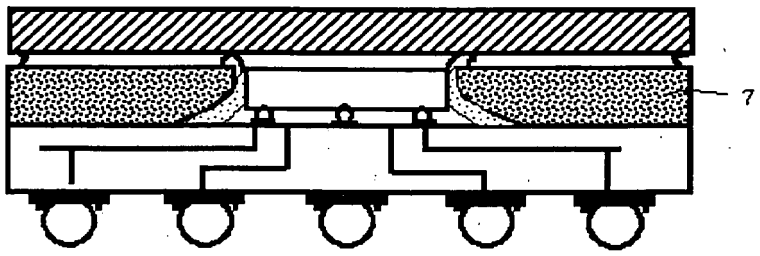


【図７】
Fig. 7

(a)

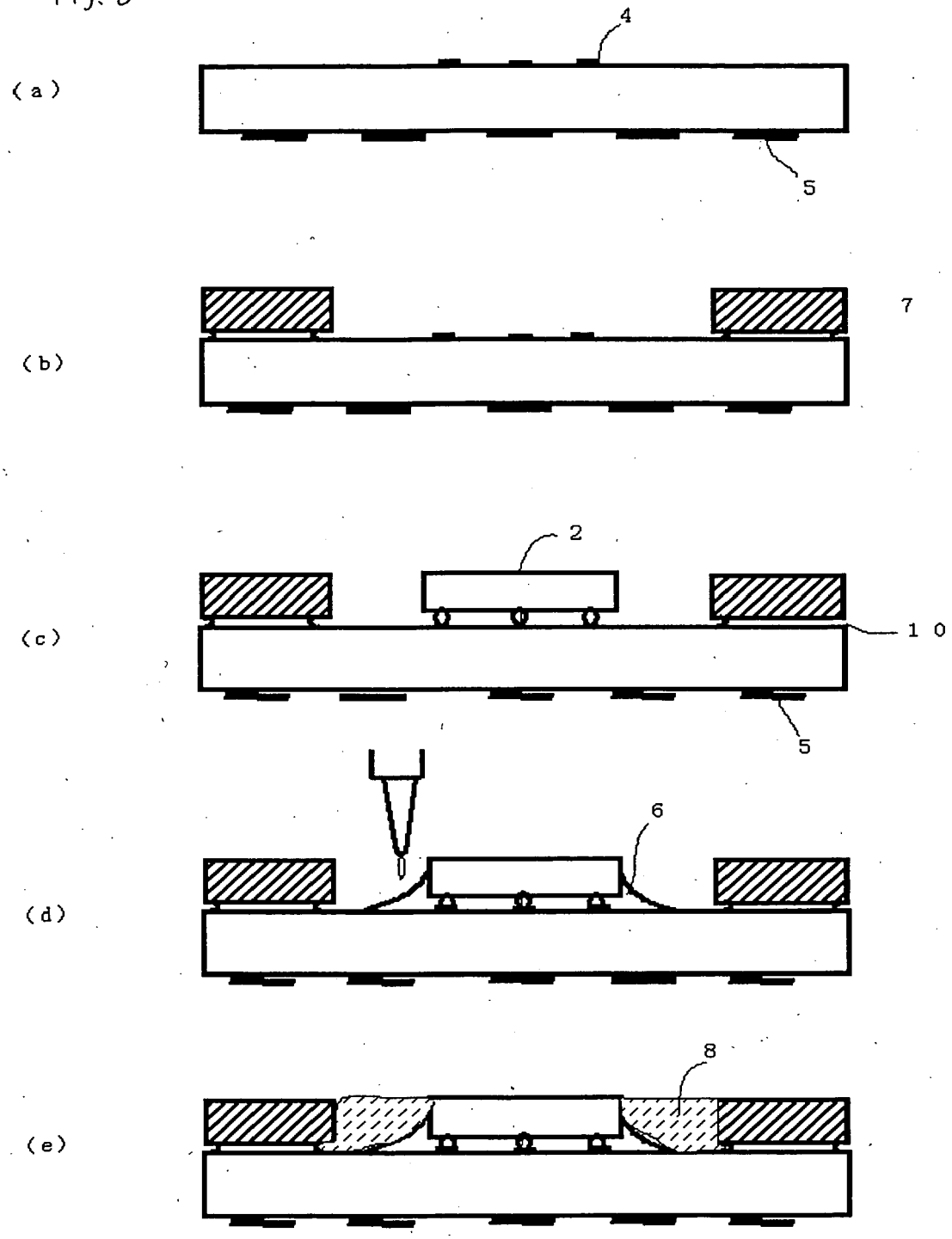


(b)

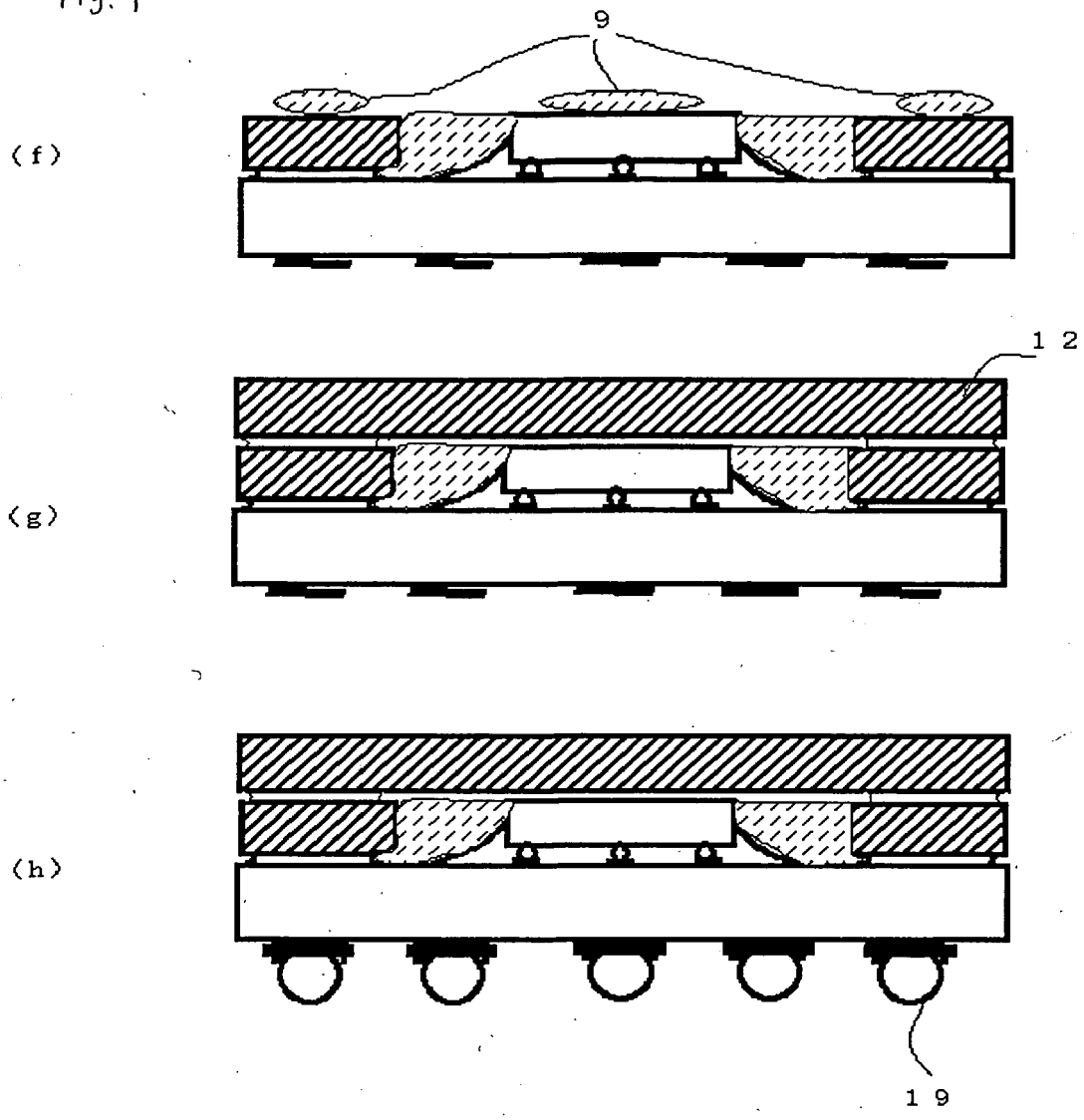


BEST AVAILABLE COPY

【図８】
Fig. 8



【図９】
Fig.9

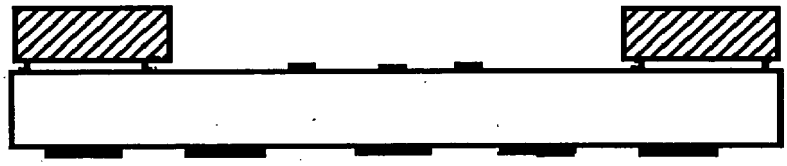


BEST AVAILABLE COPY

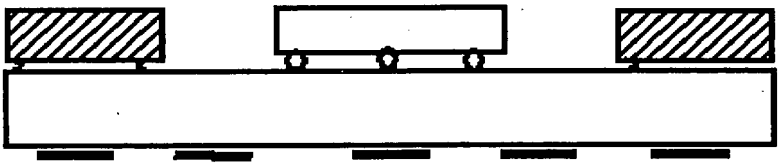
【図１０】
Fig. 10

(a)

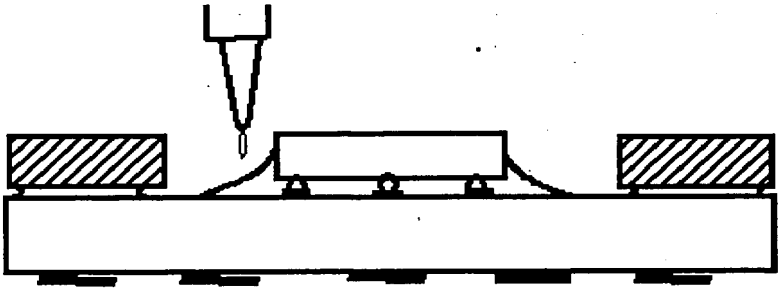
(b)



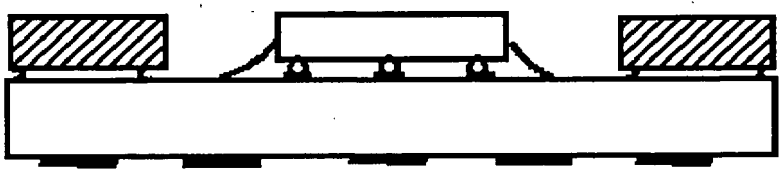
(c)



(d)

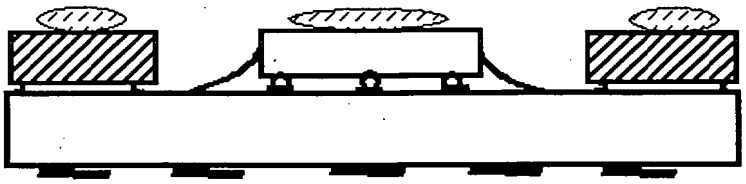


(e)

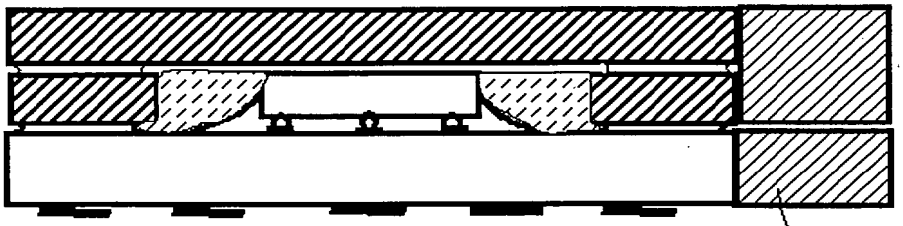


【図１１】
Fig. 11

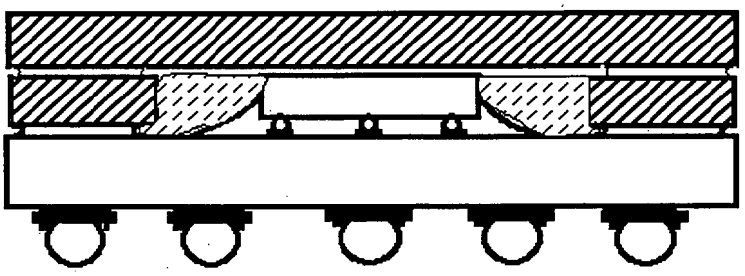
(f)



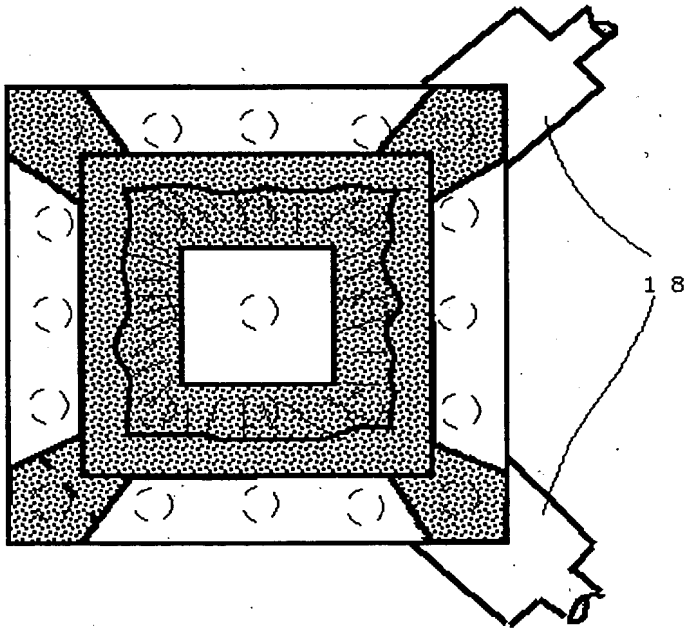
(g)



(h)



(i)



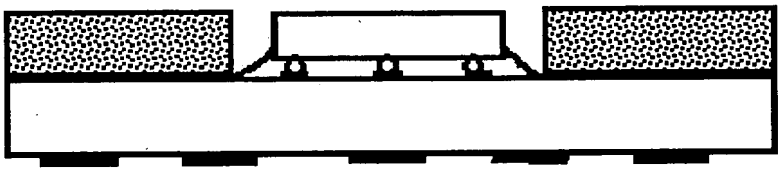
BEST AVAILABLE COPY

【図１２】
Fig. 12

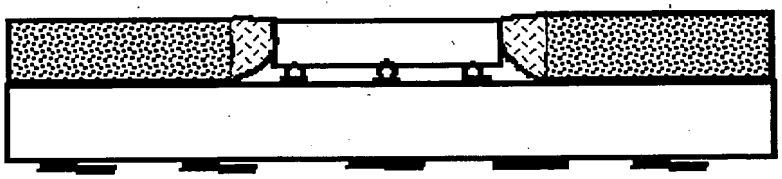
(a)

(b)

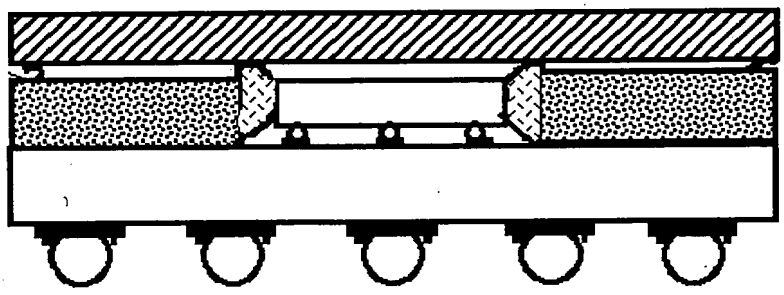
(c)



(d)



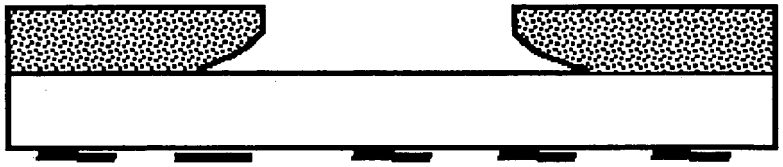
(f)



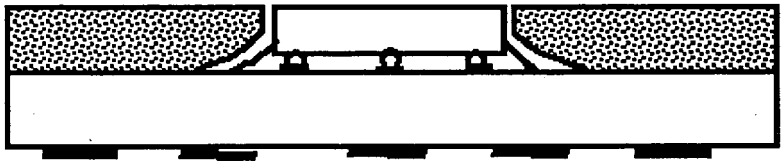
【図１３】
Fig. 13

(a)

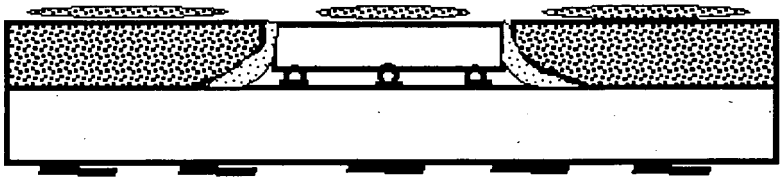
(b)



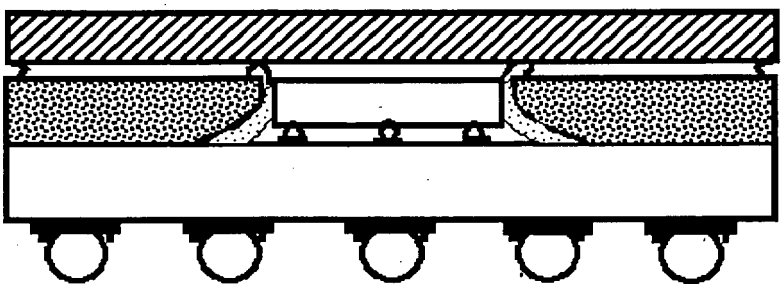
(c)



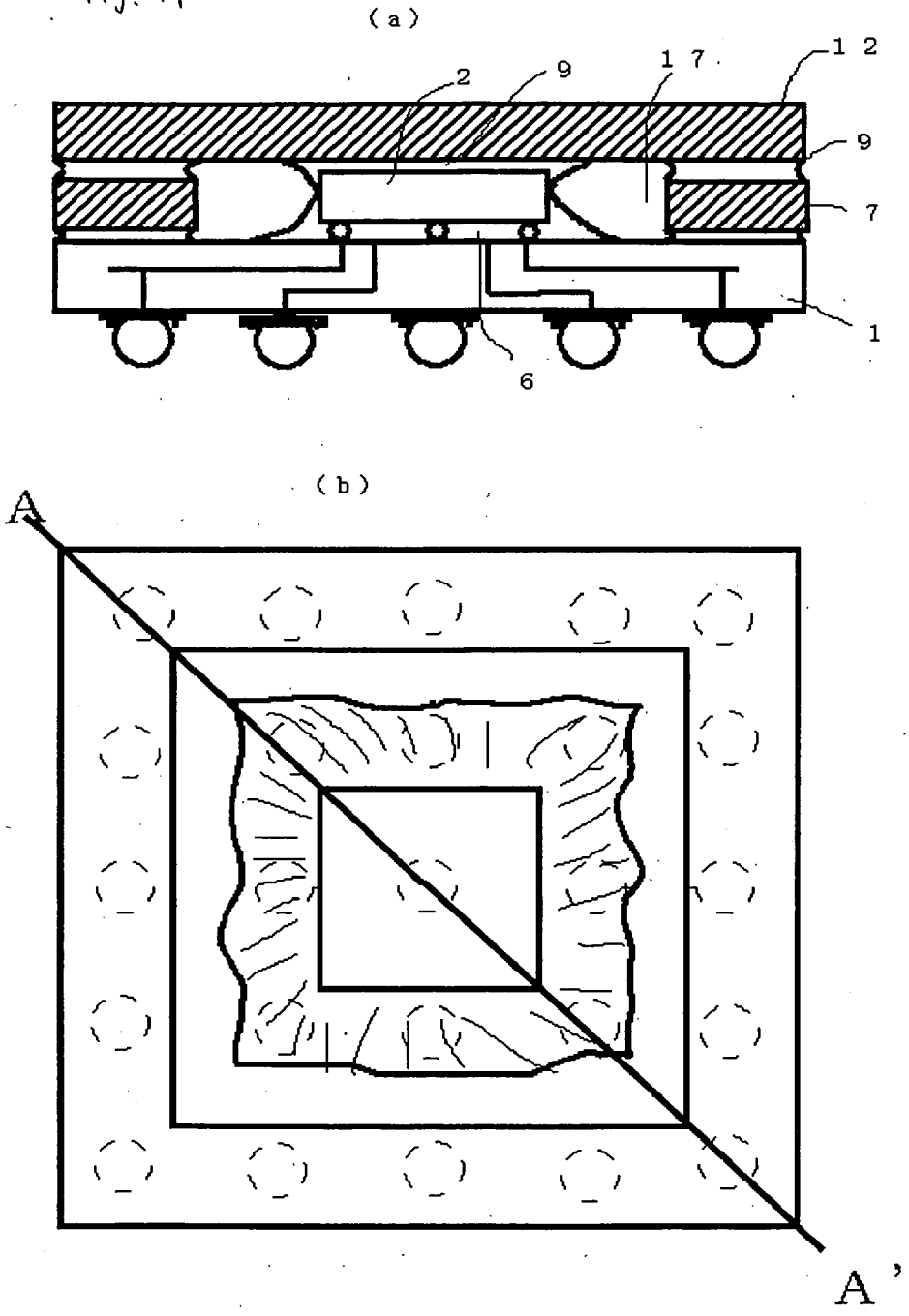
(d)



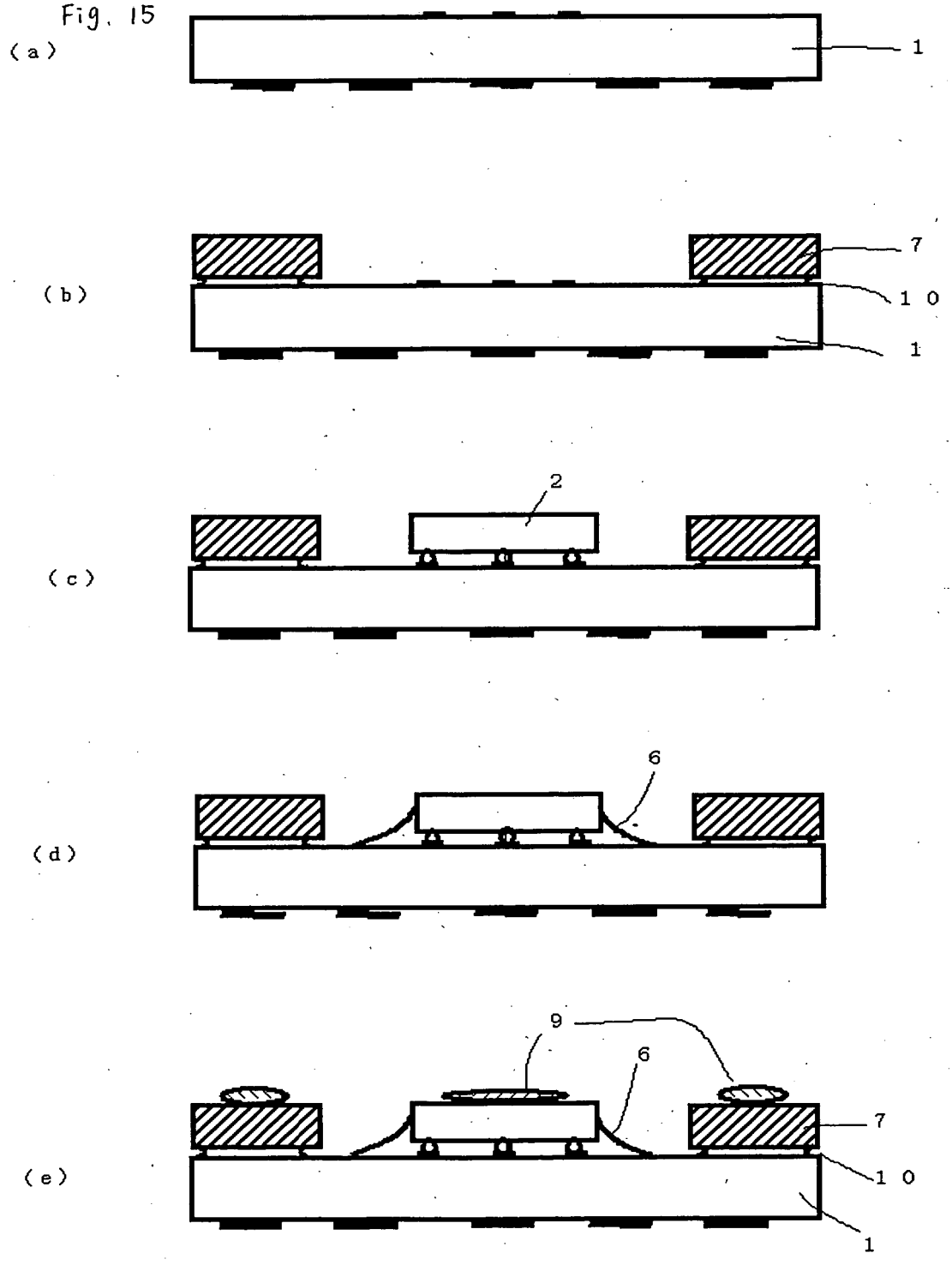
(e)



【図１４】
Fig. 14

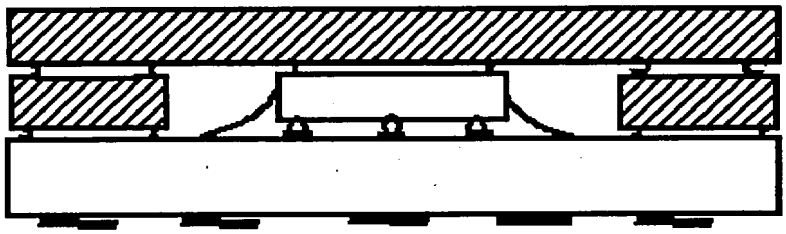


【図１５】
Fig. 15

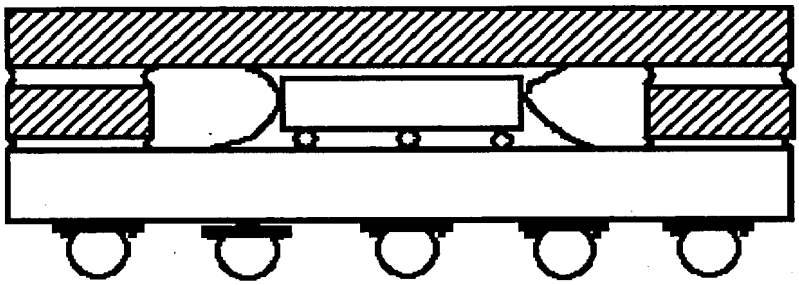


【図１６】
Fig. 16

(f)

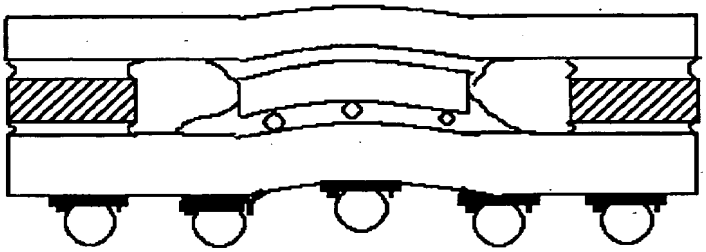


(g)



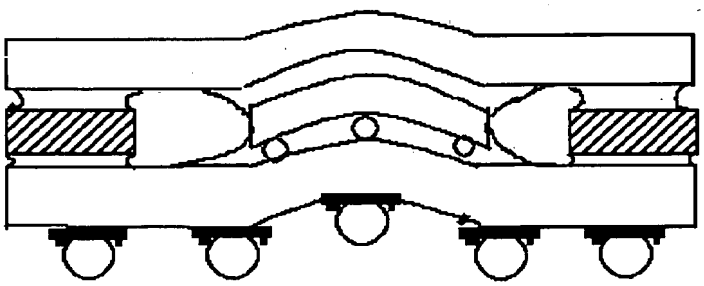
【図１７】
Fig. 17

(a)



常温状態
２０℃
CONDITION AT
NORMAL TEMPERATURE

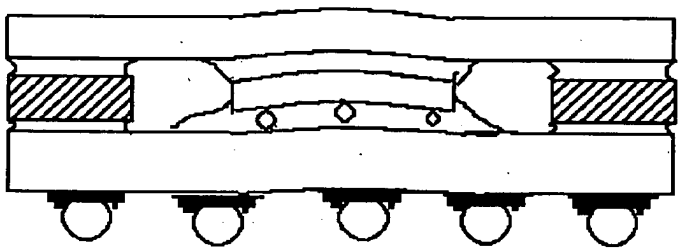
(b)



冷却状態
－４５℃
COOLED CONDITION

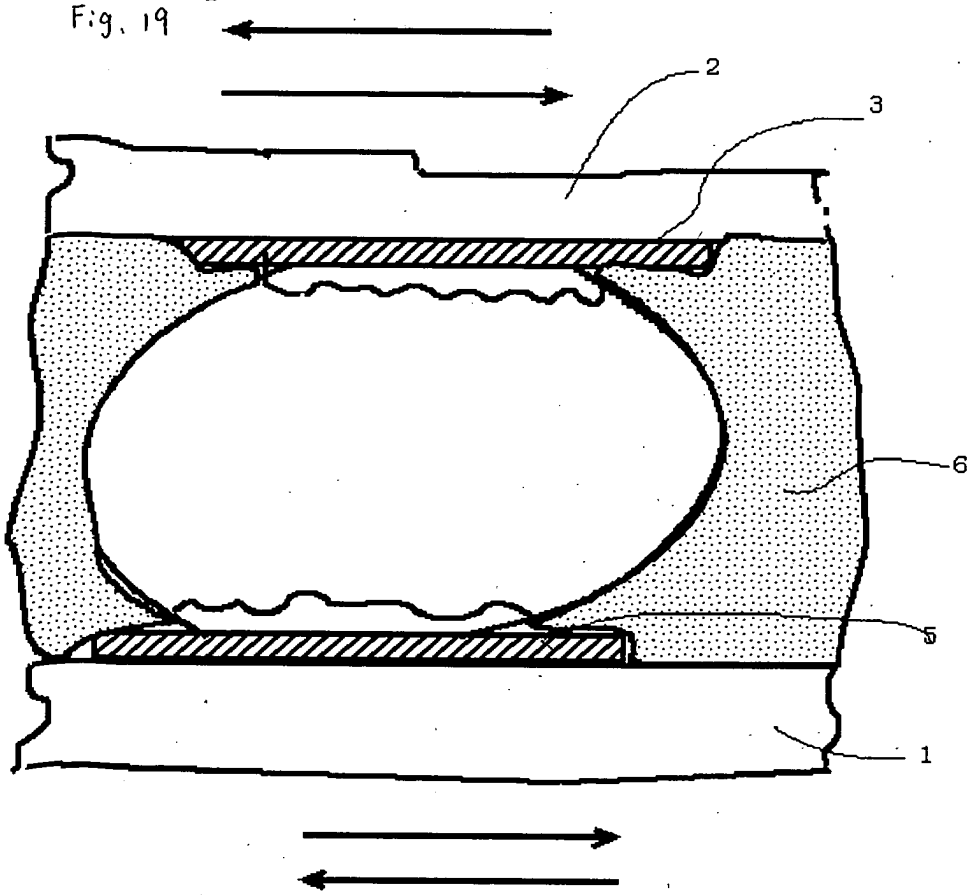
【図１８】
Fig.18

(c)



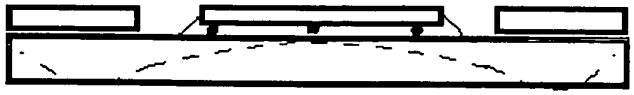
過熱状態
１５０℃
OVERHEATED CONDITION

【図１９】
Fig. 19

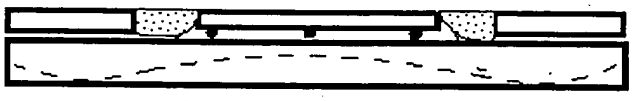


【図２０】
Fig. 20

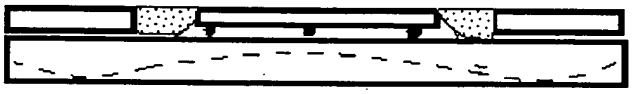
（a）従来
CONVENTIONAL



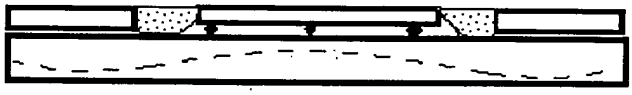
（b）第１実施例
FIRST EXAMPLE



（c）第２実施例
SECOND EXAMPLE

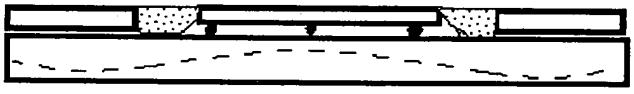


（d）第３実施例
THIRD EXAMPLE

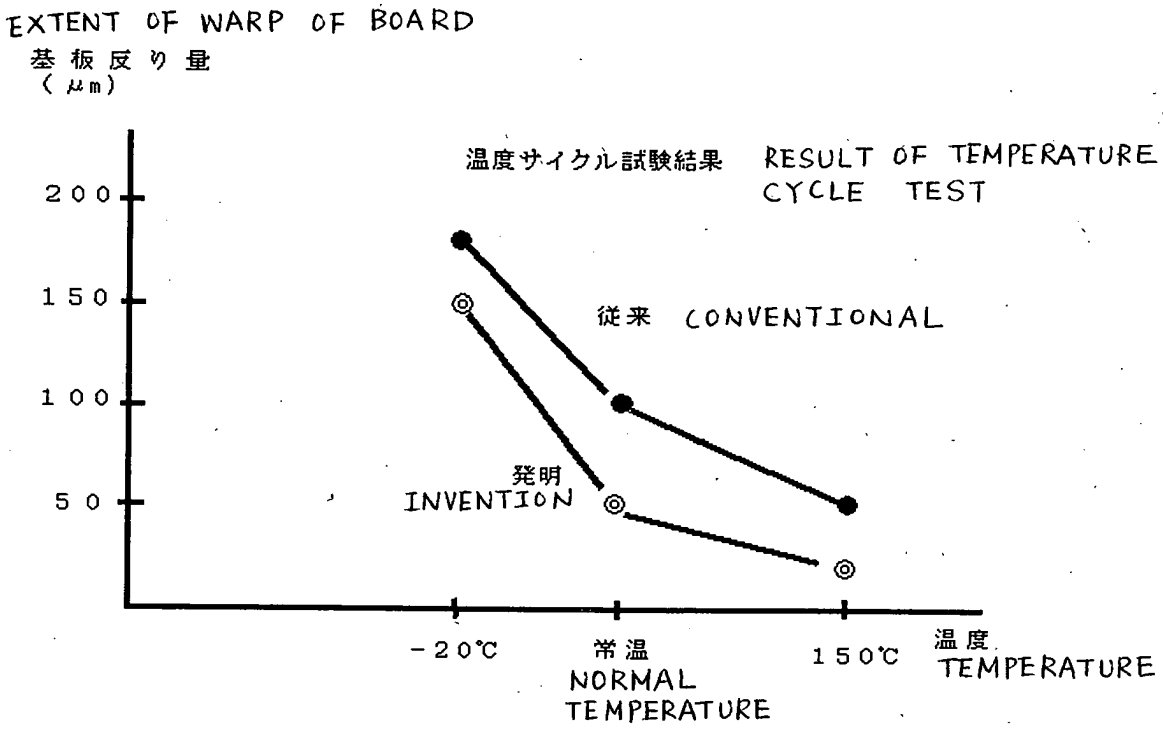


（e）第４実施例
FOURTH EXAMPLE

（f）第５実施例
FIFTH EXAMPLE



【図２１】
Fig. 21


EXTENT OF WARP OF BOARD
基板反り量
（μm）
温度サイクル試験結果　RESULT OF TEMPERATURE CYCLE TEST
２００
１５０
１００
５０
従来　CONVENTIONAL
発明
INVENTION
－２０℃
常温
NORMAL TEMPERATURE
１５０℃
温度
TEMPERATURE

[Document Name] Abstract

[Abstract]

[Problem]

To provide a semiconductor device, in which: its wiring board is prevented from warping; its solder bumps are prevented from cracking; and its lands are prevented from being separated from its wiring board, in a case where a semiconductor chip is connected to the wiring board through flip chip bonding, and in a case where an underfill resin is filled in the interstice between the wiring board and semiconductor chip, followed by hardening.

[Solving Means]

The semiconductor chip is connected to the wiring board through flip chip bonding; the underfill resin is filled in the interstice between the wiring board and the semiconductor chip, followed by hardening; and a resin which has a coefficient of thermal expansion lower than that of the underfill resin is filled in a gap surrounded by a reinforcement frame (stiffener) encompassing the semiconductor chip and a lid for protecting the semiconductor device, followed by hardening.

[Selected Drawing] Fig. 1